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(54) **Semiconductor memory circuit having shift redundancy circuits**

Halbleiterspeicheranordnung mit Schieberedundanzschaltungen

Dispositif de mémoire à semiconducteur ayant des circuits de redondance par déclalage

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Description

[0001] The present invention relates to a semiconductor memory circuit, and specifically to a semiconductor memory circuit having shift redundancy circuits used for substituting a redundancy memory cell for a defective memory cell.

[0002] Recently, remarkable developments have been made in a semiconductor memory circuit as a result of an improved technique of forming fine semiconductor elements, and an accessing speed of writing and reading data has been increased.

[0003] However, if the access speed is accelerated as described above, especially in the case of a synchronous semiconductor memory circuit, in the conventional redundancy circuit of a redundancy memory cell substituting type, selecting speeds of the redundancy memory cell and a normal memory cell become different from each other when the redundancy memory cell is substituted for the normal memory cell. Therefore, there is a tendency to use a shift redundancy circuit which does not generate a difference in selecting speed of the redundancy and normal memory cells.

[0004] Fig. 1 is a block diagram showing a conventional semiconductor memory circuit of the redundancy memory cell substituting type having the shift redundancy circuits.

[0005] Memory cell arrays MC11 to MC18 and a redundancy memory cell array MCR1 are connected to corresponding sense amplifier/write buffers SA11 to SA18 and SAR1 through corresponding column decoders YS11 to YS18 and YSR1 when the column decoders are selected.

[0006] An input/output signal line WA11 connected to the sense amplifier/write buffer SA11 and an input/output signal line WA12 connected to the sense amplifier/write buffer SA12 are connected to input terminals of a shift redundancy circuit SF11.

[0007] Similarly, input/output signal lines WA12 to WA18 and WAR1 respectively connected to the sense amplifier/write buffers SA12 to SA18 and SAR1 are connected to input terminals of shift redundancy circuits SF12 to SF18. Switch signal lines FS11 to FS18 to which fuse elements FA11 to FA18 on an output line of a program circuit PR11 are connected to the shift redundancy circuits SF11 to SF18, and the switch signal lines FS11 to FS18 are connected to a control terminal.

[0008] In the program circuit PR11, a fuse element FAP1 and a resistance element R11 are connected to each other in series between a power supply potential VCC and a ground potential GND. A potential of a node between the fuse element FAP1 and the resistance element R11 is output to the fuse elements FA11 to FA18 through inverters INV13 and INV14.

[0009] A structure and an operation of the shift redundancy circuit will be described below. Fig. 2 is a circuit diagram showing the shift redundancy circuit.

[0010] The shift redundancy circuit is provided with a switch signal line FS to which a switch signal for the shift redundancy circuit is transmitted. An inverter INV5 and gates of an N-channel MOS transistor MN1 and a P-channel MOS transistor MP2 are connected to the switch signal line FS. The shift redundancy circuit is further provided with a P-channel MOS transistor MP1 having a source and a drain respectively connected to a source and a drain of the N-channel MOS transistor MN1 and an N-channel MOS transistor MN2 having a source and a drain connected to a source and a drain of the P-channel MOS transistor MP2. A gate of the P-channel MOS transistor MP1 is connected to a gate of the N-channel MOS transistor MN2 at a node, and the inverter INV5 is connected between the node and the switch signal line FS. Thus, the N-channel MOS transistor MN1 and the P-channel MOS transistor MP1 constitute a transfer-gate switch circuit TF1, and the N-channel MOS transistor MN2 and the P-channel MOS transistor MP2 constitute a transfer-gate switch circuit TF2.

[0011] Furthermore, an input/output signal line Wai is connected to one of the nodes connecting the sources and drains in the two MOS transistors of the switch circuit TF1, and an input/output signal line Wbi is connected to one of the nodes connecting the sources and drains of the two MOS transistors in the switch circuit TF2. A signal line Wci is connected to the other nodes of the switch circuits TF1 and TF2.

[0012] The switch signal line FS corresponds to the switch signal lines FS11 to FS18 in Fig. 1, and the input/output signal lines Wai and Wbi correspond to the input/output signal lines WA11 to WA18 and WAR1 in Fig. 1. The signal line Wci corresponds to signal lines OA11 to OA18 in Fig. 1.

[0013] The shift redundancy circuit formed in the above manner operates so that the switch circuit TF2 is turned off when the switch circuit TF1 is turned on, and the switch circuit TF2 is turned on when the switch circuit TF1 is turned off.

[0014] When the signal line FS is at a VCC level, for example, the switch circuit TF1 is turned on and the switch circuit TF2 is turned off. Then, a level of the signal line Wai is transmitted to the input/output signal line Wci.

[0015] When the signal line FS is at a GND level, on the other hand, the switch circuit TF1 is turned off and the switch circuit TF2 is turned on. Then, a level of the signal line Wbi is transmitted to the input/output signal line Wci.

[0016] An operation of the conventional semiconductor memory circuit in a case in which a defective memory cell array does not exist and the redundancy memory cell array is not substituted for a defective memory cell array by the shift redundancy circuit will be described below. In this case, a signal at a VCC level is output from the program circuit PR11 and the VCC level is transmitted to all of the signal lines FS11 to FS18. Then, a level of the input/output signal line WA11 is output to the signal line OA11 connected to the shift redundancy circuit SF11. Similarly, levels of the input/output signal lines

WA12 to WA18 are respectively output to the input/output signal lines OA12 to OA18.

[0017] Next, a case in which a defective memory cell array exists for which the redundancy memory cell array is substituted will be described, supposing that the memory cell array MC15 is defective. In this case, the fuse element FAP1 in the program circuit PR11 and the fuse element FA15 are cut. As a result, a signal at a GND level is output from the program circuit PR11, and the GND level is transmitted to the switch signal lines FS15 to FS 18. Then, a level of the input/output signal line WA16 is output to the signal line OA15, a level of the input/output signal line WA17 is output to the signal line OA16, a level of the input/output line WA18 is output to the signal line OA17, and a level of the input/output signal line WAR1 is output to the signal line OA18.

[0018] On the other hand, the VCC level is transmitted to the switch signal lines FS11 to FS14, even in a state in which the fuse element FA15 is cut. Consequently, output levels of the signal lines OA11 to OA14 equal the levels of the input/output signal lines WA11 to WA14, respectively.

[0019] A level of the input/output signal line WA15 corresponding to the defective memory cell array MC15 is interrupted by the shift redundancy circuits SF14 and SF15, and is not output to any of the signal lines OA14 and OA15.

[0020] In the system of substituting the redundancy memory cell using the shift redundancy circuits SF11 to SF18 as described above, a difference is not generated between speeds of selecting the redundancy memory cell and the normal memory cell. Therefore, the redundancy memory cell substituting system is used more frequently for a highspeed semiconductor memory circuit and a synchronous semiconductor memory circuit, as compared to a normal redundancy system in which a difference exists in speeds of selecting the redundancy memory cell and the normal memory cell.

[0021] However, when the shift redundancy circuits are used, whether or not the redundancy memory cell is substituted, the signal levels are transmitted to the shift redundancy circuits SF11 to SF18 by the input/output signal lines WA11 to WA18 and WAR1, as described above. As a result, because the column decoder and the sense amplifier/write buffer corresponding to the defective memory cell array keep on operating, an operating current is increased as compared with that in a normal semiconductor memory circuit.

[0022] Therefore, a semiconductor memory circuit, which is provided with killer signal generating circuits for inactivating the column decoder and the sense amplifier/write buffer connected to the defective memory cell array, is necessary.

[0023] Such a killer signal generating circuit will be described below. Fig. 3 is a circuit diagram showing the killer signal generating circuit.

[0024] In the killer signal generating circuit, a fuse element FAR and a resistance element R12 connected to each other in series are provided between a power supply potential VCC and a ground potential GND. An inverter INV15 to which another inverter INV16 is connected in series is connected to a node between the fuse element FAR and the resistance element R12. A signal line RK1 is connected to the inverter INV16.

[0025] In the killer signal generating circuit formed in the above manner, in a case in which the redundancy memory cell array is not substituted, the fuse element FAR is not cut, and the VCC level is transmitted to the signal line RK1 through the inverters INV15 and INV16. In a case in which the redundancy memory cell array is substituted, on the other hand, the fuse element FAR is cut, and the GND level is transmitted to the signal line RK1.

[0026] Fig. 4 is a block diagram showing a conventional redundancy memory cell substituting semiconductor memory circuit having killer signal generating circuits and shift redundancy circuits. In the prior art shown in Fig. 4 (the second prior art), components similar to those in the prior art shown in Fig. 1 (the first prior art) are provided with similar reference numerals to omit detailed descriptions.

[0027] The second prior art is provided with killer signal generating circuits KR1 to KR8 and KRR for outputting killer signals EB1 to EB8 and EBR to column decoders YS11 to YS18 and YSR1 and sense amplifier/write buffers SA11 to SA18 and SAR1, respectively.

[0028] If a redundancy memory cell is not substituted, a fuse element in the killer signal generating circuit KRR is cut. As a result, the killer signal EBR acquires the GND level, and the column decoder YSR1 and the sense amplifier/write buffer SAR1 are inactivated.

[0029] On the other hand, fuse elements in the killer signal generating circuits KR1 to KR8 are not cut. For this reason, the killer signals EB1 to EB8 acquire the VCC level, and the column decoders YS11 to YS18 and the sense amplifier/write buffers SA11 to SA18 are not inactivated.

[0030] Next, a case in which a redundancy memory cell is substituted will be described. In a case in which a memory cell array MC15 is defective, for example, the fuse element in the killer signal generating circuit KR5 is cut. As a result, because the killer signal EB5 acquires the GND level, the column decoder YS15 and the sense amplifier/write buffer SA15 are inactivated.

[0031] In this manner, in the second prior art, the killer sigal generating circuits KR1 to KR8 and KRR are necessary to completely inactivate one of the column decoders YS11 to YS18 and YSR1, and one of the sense amplifier/write buffers SA11 to SA18 and SAR1 based on whether or not the defective memory cell array exists. The technique of forming a finer semiconductor memory circuit has been improved recently, as described above, and transistors constituting an internal circuit has been made finer, but fuse elements are scarcely made finer. Therefore, according to the second prior art which includes large number of fuse elements in the killer signal

generating circuits KR1 to KR8 and KRR, the size of a chip increases.

[0032] In other words, in the second prior art in which the operating current can be decreased, the fuse elements in the killer signal generating circuits can not be disposed in a layer below the signal lines and the like, but require exclusive spaces. In a case in which the size of the chip is approximately 25 mm<2>, the size of the chip increases by about 10 %.

[0033] In a case in which diffusion is conducted in a wafer of a 6-inch size, for example, if the killer signal generating circuit is not provided, a number of available pellets is 600 in a chip of 25 mm<2>, while the number of available pellets decreases by 60 per a wafer and becomes 540 in a chip of about 27.5 mm<2>, if the killer signal generating circuits are provided.

[0034] As described above, in the first prior art in which the shift redundancy circuits are used for substituting the redundancy memory cell, the operating current increases considerably, because all the column decoder and sense amplifier/write buffer circuits having the circuits which are not used operate.

[0035] The second prior art having the killer signal generating circuits for decreasing the operating current, on the other hand, suffers from a problem of an increased size of the chip.

[0036] A third prior art is described in US-A-5 146 429 wherein switching devices leads to reduction in power consumption in normal state which does not have a defective memory cell by interrupting the path from the row to reference potential with help of two switching transistor, whereby one of the transistors is ON and the other one is OFF.

[0037] The switching devices control if the fuses are cut or not but they don't bring the write/read circuit and the redundancy write/read circuit in an inactivative state when the allocated memory cell array is defective.

[0038] It is an object of the present invention to provide a semiconductor memory circuit in which a size of a chip is not increased, even in a case in which shift redundancy circuits are used for substituting a redundancy memory cell array, and an operating current can be decreased.

[0039] According to the present invention, which is defined in detail in appended claim 1, a semiconductor memory circuit having shift redundancy circuits comprises a plurality of memory cell arrays, a redundancy memory cell array to be substituted, when any one of the memory cell arrays is defective, for the defective memory cell array, a plurality of write/read circuits for writing and reading data to and from the memory cell arrays, a redundancy write/read circuit for writing and reading data to and from the redundancy memory cell array, a plurality of shift redundancy circuits each connected to two of the write/read circuits and the redundancy write/read circuit. The shift redundancy circuit each allows one of signals output from the two circuits to pass through. The semiconductor memory circuit comprises a plurality of fuse elements connected to each other in series. One of the fuse elements is connected between one of the shift redundancy circuits and a power supply potential, and the others of the fuse elements are respectively connected between two of the shift redundancy circuits. Furthermore, the semiconductor memory circuit comprises a program circuit connected to one of the fuse elements disposed at an end portion opposite to the fuse element connected to the power supply potential and a plurality of cut fuse detecting circuits. The program circuit selectively outputs a power supply potential or a ground potential. The cut fuse detecting circuit each detects individually whether each of the fuse elements is cut or not and controls each of the write/read circuit and the redundancy write/read circuit in an activated state or a inactivated state, based on a result of the detection.

[0040] Because the present invention is provided with the cut fuse detecting circuits for individually detecting whether the fuse elements are cut or not and for controlling each of the write/read circuits and the redundancy write/read circuit in the activated state or the inactivated state, according to the result of the detection, the write/read circuit allocated to the defective memory cell array can be brought into the inactivated state. In this manner, an operating current can be decreased.

[0041] Also, because the cut fuse detecting circuits can be formed without using fuse elements and can be disposed in a layer below the signal lines, increase in size of the chip can be prevented. Therefore, it is possible to prevent decrease in a number of available pellets per a wafer.

Fig. 1 is a block diagram showing a conventional semiconductor memory circuit of a redundancy memory cell substituting system having shift redundancy circuits;

Fig. 2 is a circuit diagram showing the shift redundancy circuit;

Fig. 3 is a circuit diagram showing a killer signal generating circuit;

Fig. 4 is a block diagram showing a conventional semiconductor memory circuit of a redundancy memory cell substituting system having the killer signal generating circuits and the shift redundancy circuits; and

Fig. 5 is a block diagram showing an embodiment of a semiconductor memory circuit according to the present invention.

[0042] An embodiment of a semiconductor memory circuit according to the present invention will be specifically described below with reference to accompanying drawings. Fig. 5 is a block diagram showing the embodiment of the semiconductor memory circuit of the present invention.

[0043] The present embodiment is provided with eight memory cell arrays MC1 to MC8 and a redundancy

memory cell array MCR. The embodiment is further provided with column decoders YS1 to YS8 and a redundancy column decoder YSR respectively connected to pairs of bit lines (not shown) of the memory cell arrays MC1 to MC8 and the redundancy memory cell array MCR. Furthermore, sense amplifier/write buffers SA1 to SA8 and a redundancy sense amplifier/write buffer SAR are respectively connected to the column decoders YS1 to YS8 and the redundancy column decoder for inputting written data and amplifying read data. Input/output signal lines WA1 to WA8 and a redundancy input/output signal line WAR are respectively connected to the sense amplifier/write buffers SA1 to SA8 and the redundancy sense amplifier/write buffer SAR.

[0044] A shift redundancy circuit SF1 is connected to the input/output signal lines WA1 and WA2, a shift redundancy circuit SF2 is connected to the input/output signal lines WA2 and WA3, and shift redundancy circuits SF3 to SF7 are similarly connected to the input/output signal lines WA3 to WA8. Further, a shift redundancy circuit SF8 is connected to the input/output signal line WA8 and the redundancy input/output signal line WAR. Signals output from the shift redundancy circuits SF1 to SF8 are respectively transmitted to the signal lines OA1 to OA8.

[0045] The shift redundancy circuit SF1 alternatively selects one of signals output from the sense amplifier/write buffers SA1 and SA2 as a control signal and outputs the result to the signal line OA1. Similarly, the shift redundancy circuits SF2 to SF8 output selection results to the signal lines OA2 to OA8. Switch signal lines FS1 to FS8 are connected to the shift redundancy circuits SF1 to SF8. A fuse element FA1 is provided between the switch signal line FS1 and a power supply potential VCC. A fuse element FA2 is provided between the switch signal line FS1 and the switch signal line FS2. Similarly to the fuse element FA2, fuse elements FA3 to FA8 are provided between two of the switch signal lines FS2 to FS8.

[0046] Furthermore, the present embodiment is provided with a program circuit PR1 having a switch fuse element FAP and a resistance element R1 connected in series to each other between a power supply potential VCC and a ground potential GND. In the program circuit PR1, an inverter INV3 is connected to a node between the switch fuse element FAP and the resistance element R1, and another inverter INV4 is connected to the inverter INV3 in series. The inverter INV4 is connected to the switch signal line FS8.

[0047] Also a cut fuse detecting circuit FK2 is provided which has two input terminals into which potentials of opposite terminals of the fuse element FA2 are input. The cut fuse detecting circuit FK2 comprises a NAND circuit NA and an inverter circuit INV1 connected to one of input terminals of the NAND circuit NA. A potential of a node between the fuse element FA1 and the fuse element FA2 is input into the other input terminal of the NAND circuit NA. A potential of a node between the fuse element FA2 and the fuse element FA3 is input into the inverter INV1. Similarly to the cut fuse detecting circuit FK2, potentials of opposite terminals of each of the fuse elements FA3 to FA8 are input into two input terminals of each of the cut fuse detecting circuits FK3 to FK8. In other words, the potential of the corresponding fuse element on the side of the program circuit PR1 is input into the input terminal of the cut fuse detecting circuit provided with the inverter, while the potential of the corresponding fuse element on the side of the power supply potential VCC is input into the input terminal of the cut fuse detecting circuit which is not provided with the inverter.

[0048] The potential of the node between the fuse element FA1 and the fuse element FA2 functioning as a killer signal EA1 controls an activated/inactivated state of the column decoder YS1 and the sense amplifier/write buffer SA1 constituting a write/read circuit. Killer signals EA2 to EA8 output from the cut fuse detecting circuits FK2 to FK8 control activated/inactivated states of the column decoders YS2 to YS8 and the sense amplifier/write buffers SA2 to SA8 constituting write/read circuits.

[0049] An inverter INV2 is connected among the program circuit PR1 and the redundancy column decoder YSR, and the redundancy sense amplifier/write buffer SAR. A signal output from the program circuit PR1 and inverted by the inverter INV2 controls an activated/inactivated state of the redundancy column decoder YSR and the redundancy sense amplifier/write buffer SAR constituting a redundancy write/read circuit.

[0050] Some repeated portions are omitted in Fig. 5 to make the drawing less complicated. The components can be repeated, if necessary.

[0051] For better understanding, an operation of the present embodiment having the above structure will be schematically described.

[0052] In a case in which one of the memory cell arrays MC1 to MC8 is defective and the redundancy memory cell array MCR is to be substituted for the defective memory cell array, one of the fuse elements FA1 to FA8 corresponding to the defective memory cell array and the switch fuse element FAP in the program circuit PR1 are cut. When the switch fuse element FAP in the program circuit PR1 is cut, a signal at a GND level is output from the program circuit PR1, and the GND level is transmitted to one terminal of the fuse element cut corresponding to the defective memory cell array. On the other hand, a VCC level is transmitted from the power supply potential VCC to the other terminal of the cut fuse element and to the fuse elements between the cut fuse and the power supply potential VCC.

[0053] Therefore, the different potentials, i.e., the VCC level and the GND level are respectively transmitted to the opposite terminals of the cut fuse elements, while the same potential is transmitted to the opposite terminals of the fuse elements which are not cut.

[0054] Input ends of the cut fuse detecting circuits

FK1 to FK8 are connected to the opposite ends of the fuse elements FA2 to FA8 (switch signal lines FS2 to FS8). If different potentials are input respectively into the opposite terminals of the corresponding fuse element, the corresponding column decoder and sense amplifier/ write buffer are inactivated by the cut fuse detecting circuit. If the same potential are input respectively into the opposite terminals of the corresponding fuse element, the corresponding column decoder and sense amplifier/ write buffer are activated by a signal output from the cut fuse detecting circuit. Thus, an operating current can be decreased by inactivating the circuits corresponding to the defective one of the memory cell arrays MC1 to MC8.

[0055] Next, the operation of the present embodiment will be specifically described.

[0056] As described above, the switch signal lines FS1 and FS2 are connected to the input terminals of the cut fuse detecting circuit FK2. If both of the switch signal lines FS1 and FS2 are at the VCC level, a killer signal EA2 at the VCC level is output from the cut fuse detecting circuit FK2, because one of the input terminals of the NAND circuit NA (an output from the inverter INV1) acquires the GND level. Also in a case in which both of the switch signal lines FS1 and FS2 are at the GND level, the killer signal EA2 acquires the VCC level.

[0057] On the other hand, if the switch signal line FS1 is at the VCC level and the switch signal line FS2 is at the GND level, the killer signal EA2 acquires the GND level.

[0058] Similarly to the cut fuse detecting circuit FK2, when potentials of both of the signal lines of the fuse element corresponding to the cut fuse detecting circuits FK3 to FK8 are at the VCC level or the GND level, the killer signals EA3 to EA8 are at the VCC level. When one of the signal lines of the fuse element corresponding to each of the cut fuse detecting circuits FK3 to FK8 is at the GND level and the other is at the VCC level, each of the killer signals EA3 to EA8 acquires the GND level.

[0059] Next, an operation in a case in which a defective memory cell array does not exist and the redundancy memory cell array is not substituted for any of the memory cell arrays will be described. In the case in which the redundancy memory cell array is not substituted, all switch signal lines FS1 to FS8 are at the VCC level, because the switch fuse element FAP is not cut in the program circuit PR1.

[0060] In this case, a signal at the VCC level is output from the program circuit PR1. Because the inverter INV2 is connected between the redundancy column decoder YSR and the redundancy sense amplifier/write buffer SAR for the redundancy memory cell and the program circuit PR1, the killer signal EAR at the GND level is transmitted to the redundancy column decoder YSR and the redundancy sense amplifier/write buffer SAR. The redundancy column decoder YSR and the redundancy sense amplifier/write buffer SAR for the redundancy memory cell are inactivated, thereby decreasing the operating current.

[0061] On the other hand, because the switch signal lines FS1 to FS8 to which signals input into the cut fuse detecting circuits FK2 to FK8 are transmitted are at the VCC level, the killer signals EA2 to EA8 are at the VCC level. At this time, the column decoders YS2 to YS8 and the sense amplifier/write buffers SA2 to SA8 are activated.

[0062] Since the killer signal EA1 acquires the VCC level which is the same as the level of the switch signal line FS1, the column decoder YS1 and the sense amplifier/write buffer SA1 are also activated.

[0063] Next, a case in which a defective memory cell array exists, for which the redundancy memory cell array is substituted will be described, supposing that the memory cell array 5 is defective. In this case, the switch fuse element FAP in the program circuit PR1 and the fuse element FA5 are cut. As a result, the program circuit PR1 outputs a signal at the GND level, and the GND level is transmitted to the switch signal lines FS5 to FS8. To the switch signal lines FS1 to FS4, on the other hand, the VCC level is transmitted.

[0064] At this time, in the cut fuse detecting circuit FK5, the switch signal line FS4 which is one input line of the cut fuse detecting circuit FK5 is at the VCC level, while the switch signal line FS5 which is the other input line is at the GND level. Because the killer signal EA5 output from the cut fuse detecting circuit FK5 is at the GND level, the column decoder YS5 and the sense amplifier/write buffer SA5 are inactivated, thereby decreasing the operating current.

[0065] On the other hand, the switch signal lines FS1 to FS4 which are the input lines of the cut fuse detecting circuits FK2 to FK4 are at the VCC level. Therefore, the killer signals EA2 to EA4 acquire the VCC level and the column decoders YS2 to YS4 and the sense amplifier/ write buffers SA2 to SA4 are activated.

[0066] Since the killer signal EA1 is at the VCC level similarly to the switch signal line FS1, the column decoder YS1 and the sense amplifier/write buffer SA1 are activated.

[0067] Further, because the GND level is input into the cut fuse detecting circuits FK6 to FK8, the killer signals EA6 to EA8 acquire the VCC level. Consequently, the column decoders YS6 to YS8 and the sense amplifier/ write buffers SA6 to SA8 are activated.

[0068] Moreover, since the signal at the GND level output from the program circuit PR1 is input into the inverter INV2 and is inverted, the killer signal EAR corresponding to the redundancy memory cell array MCR acquires the VCC level. As a result, the redundancy column decoder YSR and the redundancy sense amplifier/ write buffer SAR for the redundancy memory cell are activated.

[0069] Next, an operation in a case in which the memory cell array MC1 is defective will be described. In this case, the switch fuse element FAP in the program circuit PR1 and the fuse element FA1 are cut. As a result, an

output signal from the program circuit PR1 is at the GND level, and all the switch signal lines FS1 to FS8 acquire the GND level.

[0070] At this time, signals at the GND level are input into both of the input terminals of the cut fuse detecting circuits FK2 to FK8, and the killer signals EA2 to EA8 acquire the VCC level. Consequently, the column decoders YS2 to YS8 and the sense amplifier/write buffers SA2 to SA8 are activated.

[0071] Because the signal at the GND level output from the program circuit PR1 is input into the inverter INV2 and inverted, the killer signal EAR corresponding to the redundancy memory cell array MCR acquires the VCC level. Therefore, the redundancy column decoder YSR and the redundancy sense amplifier/write buffer SAR for the redundancy memory cell are activated.

[0072] On the other hand, because the killer signal EA1 is at the GND level similarly to the switch signal line FS1, the column decoder YS1 and the sense amplifier/write buffer SA1 are inactivated, thereby decreasing the operating current.

[0073] In this manner, the present embodiment is provided with the cut fuse detecting circuits FK2 to FK8 for detecting whether or not the fuse elements FA1 to FA8 for shift redundancy treatment are cut, and generating the killer signals EA1 to EA8 and EAR according to the detection results, thereby decreasing the operating current without increasing the size of the chip.

[0074] The structure of the cut fuse detecting circuit is not limited to the circuit having the NAND circuit and the inverter circuit connected to each other. The cut fuse detecting circuit may be composed of any logic circuits which can detect a difference between the potentials of the opposite terminals of the cut fuse connected to the shift redundancy circuit.

[0075] According to the first prior art, nine sets of column decoders and sense amplifier/write buffers operate to transmit the level of the input/output signal lines to the shift redundancy circuits, whether or not the redundancy memory cell array is substituted. As a result, the operating current of the entire circuit is "9i" ampere, supposing that the operating current of a set of the column decoder and the sense amplifier/write buffer is "i" ampere.

[0076] In contrast, according to the present embodiment, the operating current is "8i" ampere, which is 15 % less than that of the first prior art.

[0077] Furthermore, the cut fuse detecting circuits can be formed without using the fuse elements and can be disposed in a layer below the respective signal lines, thereby preventing an increase of the chip size. Therefore, it is possible to prevent a decrease in the number of the available pellets per a wafer.

Claims

1. A semiconductor memory circuit having shift redundancy circuits comprises:

   a plurality of memory cell arrays (MC1 to MC8);

   a redundancy memory cell array (MCR) to be substituted, when any one of said memory cell arrays (MC1 to MC8) is defective, for said defective memory cell array;

   a plurality of write/read circuits (YS1 to YS8 and SA1 and SA8) for writing and reading data to and from said memory cell arrays (MC1 to MC8);

   a redundancy write/read circuit (YSR and SAR) for writing and reading data to and from said redundancy memory cell array (MCR);

   a plurality of shift redundancy circuits (SF1 to SF8) each connected to two of said write/read circuits (YS1 to YS8 and SA1 to SA8) and said redundancy write/read circuit (YSR and SAR), said shift redundancy circuits (SF1 to SF8) allowing one of the signals output from said two circuits (YS1 to YS8 and SA1 to SA8) to pass through;

   a plurality of fuse elements (FA1 to FA8) connected to each other in series, one of said fuse elements (FA1) being connected between one of said shift redundancy circuits (SF1) and a power supply potential (VCC), and the others of said fuse elements (SF2 to SF8) being respectively connected between two of said shift redundancy circuits (SF1 to SF8);

   a program circuit (PR1) connected to one of said fuse elements disposed at an end portion (FA8) opposite to said fuse element connected to said power supply potential (FA1), said program circuit (PR1) selectively outputting a power supply potential or a ground potential;

   a plurality of cut fuse detecting circuits (FK2 to FK8) for individually detecting whether said fuse elements (FA2 to FA8) are cut or not,

   and whereby each of said cut fuse detecting circuits controls each of said write/read circuits (YS1 to YS8 and SA1 to SA8) and said redundancy write/read circuit (YSR and SAR) to be in an activated state or in an inactivated state, based on a result of the detection, and that, according to the result of detection, the write/read circuit allocated to the defective memory cell array is brought into an inactivated state.

2. A semiconductor memory circuit according to claim

1, whereby

said write/read circuits (YS1 to YS8 and SA1 to SA8) each comprises:

a column decoder (YS1 to YS8) connected to one of said memory cell arrays (MC1 to MC8); and
a sense amplifier/write buffer (SA1 to SA8) connected to said column decoder (YS1 to YS8), and

said redundancy write/read circuit (YSR and SAR) comprises:

a redundancy column decoder (YSR) connected to said redundancy memory cell array (MCR); and
a redundancy sense amplifier/write buffer (SAR) connected to said redundancy column decoder (MCR).

3. A semiconductor memory circuit according to claim 1, whereby said program circuit (PR1) comprises a switch fuse element (FAP) connected between a power supply potential (VCC) and a ground potential and selectively outputs said power supply potential (VCC) or said ground potential according to whether said switch fuse element (FAP) is cut or not.

4. A semiconductor memory circuit according to claim 1, whereby said cut fuse detecting circuits (FK2 to FK8) are connected to opposite terminals of said fuse elements (FA2 to FA8) and detect whether said fuse elements (FA2 to FA8) are cut or not, according to a difference between potentials of said opposite terminals of said fuse elements (FA2 to FA8).

5. A semiconductor memory circuit according to claim 1, further comprising signal lines (FS1 to FS8) for connecting said shift redundancy circuit (SF1 to SF8) and said cut fuse detecting circuits (FK2 to FK8), said cut fuse detecting circuits (FK2 to FK8) being formed in a layer lower than a layer in which said signal lines are formed.

6. A semiconductor memory circuit according to claim 1, whereby said cut fuse detecting circuits (FK2 to FK8) each comprises:

an inverter (INV1) connected to a terminal of said fuse element (FA2 to FA8) on a side of said program circuit (PR1), and
a logic circuit (NA) to which a potential of a terminal of said fuse element (FA2 to FA8) on a side of said power supply potential (VCC) and a potential output from said inverter (INV1) are input.

7. A semiconductor memory circuit according to claim 1, whereby said cut fuse detecting circuits (FK2 to FK8) are respectively connected to a second and succeeding ones of said fuse elements (FA2 to FA8) from said power supply potential (VCC).

8. A semiconductor memory circuit according to claim 1, whereby said cut fuse detecting circuits (FK2 to FK8) interrupt a power current of said write/read circuit (YS1 to YS8 and SA1 to SA8) to which a cut one of said fuse elements (FA1 to FA8) is allocated.

9. A semiconductor memory circuit according to claim 3, whereby said program circuit (PR1) comprises:

a resistor (R1) connected between said switch fuse element (FAP) and said ground potential;
a first inverter (INV3) connected to a node connecting said switch fuse element (FAP) and said resistor (R1); and
a second inverter (INV4) connected to said first inverter (INV3) in series.

10. A semiconductor memory circuit according to claim 1, whereby said shift redundancy circuits (SF1 to SF8) each comprises:

a first switch circuit (TF1) which is conducting when said fuse element (FA1 to FA8) allocated to said shift redundancy circuit (SF1 to SF8) is cut and is non-conducting when said fuse element (SF1 to SF8) is not cut; and
a second switch circuit (TF2) which is non-conducting when said fuse element (SF1 to SF8) allocated to said shift redundancy circuit is cut and is conducting when said fuse element (SF1 to SF8) is not cut.

Patentansprüche

1. Halbleiter-Speicherschaltkreis mit einem Schiebe-Redundanzschaltkreis, welcher Folgendes aufweist:

eine Vielzahl von Speicherzellen-Datenfeldern (MC1 bis MC8);

ein Redundanz-Speicherzellen-Datenfeld (MCR) zum Austauschen eines der Speicherzellen-Datenfelder (MC1 bis MC8), wenn eines davon defekt ist;

eine Vielzahl von Schreib-/Leseschaltkreisen (YS1 bis YS8 und SA1 bis SA8) zum Schreiben und Auslesen von Daten in bzw. aus den Speicherzellen-Datenfeldern (MC1 bis MC8);

einen Redundanz-Schreib-/Leseschaltkreis (YSR und SAR) zum Schreiben und Auslesen von Daten in bzw. aus dem Redundanz-Speicherzellen-Datenfeld (MCR);

eine Vielzahl von Schiebe-Redundanzschaltkreisen (SF1 bis SF8), wobei jeder Schaltkreis an zwei der Schreib-/Leseschaltkreise (YS1 bis YS8 und SA1 bis SA8) sowie an den Redundanz-Schreib-/Leseschaltkreis (YSR und SAR) angeschlossen ist, wobei es die Schiebe-Redundanzschaltkreise (SF1 bis SF8) ermöglichen, dass eines der von den beiden Schaltkreisen (YS1 bis YS8 und SA1 bis SA8) ausgegebenen Signale hindurchgelangt;

eine Vielzahl von Schmelzsicherungselementen (FA1 bis FA8), die in Reihe geschaltet sind, wobei eines der Schmelzsicherungselemente (FA1) zwischen einem der Schiebe-Redundanzschaltkreise (SF1) und einer Stromversorgungsspannung (VCC) angeschlossen ist, und die anderen Sicherungselemente (SF2 bis SF8) jeweils zwischen zwei der Schiebe-Redundanzschaltkreise (SF1 bis SF8) angeschlossen sind;

einen Programm-Schaltkreis (PR1), der mit einem der Sicherungselemente verbunden ist, das an einem Endabschnitt (FA8) angeordnet ist, der dem an die Stromversorgungsspannung (FA1) angeschlossenen Sicherungselement gegenüberliegt, wobei der Programm-Schaltkreis (PR1) wahlweise eine Stromversorgungsspannung oder eine Erdspannung ausgibt;

eine Vielzahl von unterbrochenen Schmelzsicherungs-Erfassungsschaltkreisen (FK2 bis FK8), um individuell zu erfassen, ob die Sicherungselemente (FA2 bis FA8) unterbrochen sind oder nicht,

und wobei jeder der unterbrochenen Schmelzsicherungs-Erfassungsschaltkreise jeden der Schreib-/Leseschaltkreise (YS1 bis YS8 und SA1 bis SA8) sowie den Redundanz-Schreib/Leseschaltkreis (YSR und SAR) basierend auf einem Ergebnis der Erfassung steuert, so dass sich die Schaltkreise in einem aktiven Zustand oder in einem inaktiven Zustand befinden, und dass gemäß dem Erfassungsergebnis der dem defekten Speicherzellen-Datenfeld zugeordnete Schreib-/Leseschaltkreis in einen inaktiven Zustand versetzt wird.

2. Halbleiter-Speicherschaltkreis nach Anspruch 1, wobei die Schreib-/Leseschaltkreise (YS1 bis YS8 und SA1 bis SA8) jeweils Folgendes aufweisen:

einen Spaltendecoder (YS1 bis YS8), welcher an eines der Speicherzellen-Datenfelder (MC1 bis MC8) angeschlossen ist; und
einen Leseverstärker/Schreibpuffer (SA1 bis SA8), welcher an den Spaltendecoder (YS1 bis YS8) angeschlossen ist, und wobei der Redundanz-Schreib-/Leseschaltkreis (YSR und SAR) Folgendes aufweist:

einen Redundanz-Spaltendecoder (YSR), der an das Redundanz-Speicherzellen-Datenfeld (MCR) angeschlossen ist; und

einen Redundanz-Leseverstärker/Schreibpuffer (SAR), der an den Redundanz-Spaltendecoder (MCR) angeschlossen ist.

3. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei der Programm-Schaltkreis (PR1) ein Schalt-Schmelzsicherungselement (FAP) aufweist, das zwischen einer Stromversorgungsspannung (VCC) und einer Erdspannung angeschlossen ist, und wahlweise die Stromversorgungsspannung (VCC) oder die Erdspannung ausgibt, je nachdem, ob das Schalt-Schmelzsicherungselement (FAP) ausgeschaltet ist oder nicht.

4. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei die Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis FK8) an gegenüberliegende Anschlüsse der Schmelzsicherungselemente (FA2 bis FA8) angeschlossen sind und entsprechend einem Unterschied zwischen den Spannungen der gegenüberliegenden Anschlüssen der Schmel zsicherungselemente (FA2 bis FA8) erfassen, ob die Schmelzsicherungselemente (FA2 bis FA8) geschmolzen sind oder nicht.

5. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, welcher ferner Signalleitungen (FS1 bis FS8) für das Verbinden des Schiebe-Redundanzschaltkreises (SF1 bis SF8) und der unterbrochenen Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis FK8) aufweist, wobei die unterbrochenen Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis FK8) in einer Schicht ausgebildet sind, die niedriger als die Schicht ist, in welcher die Signalleitungen ausgebildet sind.

6. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei die Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis PK8) jeweils Folgendes aufweisen:

einen Inverter (INV1), der an einen Anschluss des Schmelzsicherungselements (FA2 bis

FA8) auf einer Seite des Programm-Schaltkreises (PR1) angeschlossen ist; und

einen Logik-Schaltkreis (NA), in welchen eine Spannung eines Anschlusses des Schmelzsicherungselements (FA2 bis FA8) auf einer Seite der Stromversorgungsspannung (VCC) und ein Spannungs-Ausgangssignal aus dem Inverter (INV1) eingegeben werden.

7. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei die unterbrochenen Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis PK8) jeweils an ein zweites und nachfolgende Schmelzsicherungselemente (FA2 bis FA8) über die Stromversorgungsspannung (VCC) angeschlossen werden.

8. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei die Schmelzsicherungs-Erfassungsschaltkreise (FK2 bis FK8) einen Antriebsstrom des Schreib-/Leseschaltkreises (YS1 bis YS8 und SA1 bis SA8) unterbrechen, welchem eines der ausgeschalteten Schmelzsicherungselemente (FA1 bis FA8) zugeordnet ist.

9. Halbleiter-Speicherschaltkreis gemäß Anspruch 3, wobei der Programm-Schaltkreis Folgendes aufweist:

einen Widerstand (R1), welcher zwischen dem Umschalt-Schmelzsicherungselement (FAP) und der Erdspannung angeschlossen ist;

einen ersten Inverter (INV3), der an einen Knoten angeschlossen ist, welcher das Schalt-Schmelzsicherungselement (FAP) und den Widerstand (R1) miteinander verbindet;

einen zweiten Inverter (INV4), der mit dem ersten Inverter (INV3) in Reihe geschaltet ist.

10. Halbleiter-Speicherschaltkreis gemäß Anspruch 1, wobei die Schiebe-Redundanzschaltkreise (SP1 bis SF8) jeweils Folgendes aufweisen:

einen ersten Umschalt-Schaltkreis (TF1), welcher leitfähig ist, wenn das dem Schiebe-Redundanzschaltkreis (SF1 bis SF8) zugeordnete Schmelzsicherungselement (FA1 bis FA8) ausgeschaltet ist, und nicht leitfähig ist, wenn das Schmelzsicherungselement (SF1 bis SF8) nicht ausgeschaltet ist; und

ein zweiter Umschalt-Schaltkreis (TF2), der nicht leitfähig ist, wenn das dem Schiebe-Redundanzschaltkreis (SF1 bis SF8) zugeordnete Schmelzsicherungselement (FA1 bis FA8) ausgeschaltet ist, und leitfähig ist, wenn das Schmelzsicherungselement (SF1 bis SF8) nicht ausgeschaltet ist.

Revendications

1. Circuit mémoire à semiconducteur comportant des circuits de redondance de décalage comprenant :

une pluralité de matrices de cellules de mémoire (MC1 à MC8) ;
une matrice de cellules de mémoire de redondance (MCR) destinée à remplacer, lorsque l'une quelconque desdites matrices de cellules de mémoire (MC1 à MC8) est défectueuse, ladite matrice de cellules de mémoire défectueuse ;
une pluralité de circuits d'écriture/lecture (YS1 à YS8 et SA1 à SA8) pour écrire et lire des données vers et depuis lesdites matrices de cellules de mémoire (MC1 à MC8) ;
un circuit d'écriture/lecture de redondance (YSR et SAR) pour écrire et lire des données vers et depuis ladite matrice de cellules de mémoire de redondance (MCR) ;
une pluralité de circuits de redondance de décalage (SF1 à SF8), chacun étant connecté à deux desdits circuits d'écriture/lecture (YS1 à YS8 et SA1 à SA8) et audit circuit d'écriture/lecture de redondance (YSR et SAR), lesdits circuits de redondance de décalage (SF1 à SF8) se laissant traverser par l'un des signaux fournis en sortie par lesdits deux circuits (YS1 à YS8 et SA1 à SA8) ;
une pluralité d'éléments fusibles (FA1 à FA8) connectés entre eux en série, l'un desdits éléments fusibles (FA1) étant connecté entre l'un desdits circuits de redondance de décalage (SF1) et un potentiel d'alimentation (VCC) et les autres desdits éléments fusibles (SF2 à SF8) étant respectivement connectés entre deux desdits circuits de redondance de décalage (SF1 à SF8) ;
un circuit de programme (PR1) connecté à l'un desdits éléments fusibles disposé au niveau d'une partie d'extrémité (FA8) opposée audit élément fusible connecté audit potentiel d'alimentation (FA1), ledit circuit de programme (PR1) fournissant en sortie de façon sélective un potentiel d'alimentation ou un potentiel de masse ;
une pluralité de circuits détecteurs de fusible coupé (FK2 à FK8) pour détecter individuellement si lesdits éléments fusibles (FA2 à FA8) sont coupés ou non,
et de façon que chacun desdits circuits détecteurs de fusible coupé commande chacun desdits circuits d'écriture/lecture (YS1 à YS8 et

SA1 à SA8) et ledit circuit d'écriture/lecture de redondance (YSR et SAR) pour être dans un état activé ou dans un état inactivé, en se basant sur le résultat de la détection et en fonction du résultat de la détection, que le circuit d'écriture/lecture alloué à la matrice de cellules de mémoire défectueuse soit mis dans un état inactivé.

2. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel

lesdits circuits d'écriture/lecture (YS1 à YS8 et SA1 à SA8) comprennent chacun :

un décodeur de colonne (YS1 à YS8) connecté à l'une desdites matrices de cellules de mémoire (MC1 à MC8) ; et

un tampon d'amplificateur de lecture/d'écriture (SA1 à SA8) connecté audit décodeur de colonne (YS1 à YS8), et

ledit circuit d'écriture/lecture de redondance (YSR et SAR) comprend :

un décodeur de colonne de redondance (YSR) connecté à ladite matrice de cellules de mémoire de redondance (MCR) ; et

un tampon amplificateur d'écriture de redondance (SAR) connecté audit décodeur de colonne de redondance (MCR).

3. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel ledit circuit de programme (PR1) comprend un élément fusible de commutation (FAP) connecté entre le potentiel d'alimentation (VCC) et un potentiel de masse et fournissant de façon sélective en sortie ledit potentiel d'alimentation (VCC) ou ledit potentiel de masse en fonction du fait que ledit élément fusible de commutation (FAP) est coupé ou non.

4. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel lesdits circuits détecteurs de fusible coupé (FK2 à FK8) sont connectés aux bornes opposées desdits éléments fusibles (FA2 à FA8) et détectent si lesdits éléments fusibles (FA2 à FA8) sont coupés ou non, selon la différence entre les potentiels desdites bornes opposées desdits éléments fusibles (FA2 à FA8).

5. Circuit mémoire à semiconducteur selon la revendication 1, comprenant en outre des lignes de signaux (FS1 à FS8) pour connecter ledit circuit de redondance de décalage (SF1 à SF8) et lesdits circuits détecteurs de fusible coupé (FK2 à FK8), lesdits circuits détecteurs de fusible coupé (FK2 à FK8) étant formés dans une couche au-dessous de la couche dans laquelle sont formées lesdites lignes de signaux.

6. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel lesdits circuits détecteurs de fusible coupé (FK2 à FK8) comprennent chacun :

un inverseur (INV1) connecté à une borne dudit élément fusible (FA2 à FA8) du côté dudit circuit de programme (PR1), et

un circuit logique (NA) à l'entrée duquel sont appliqués le potentiel d'une borne dudit élément fusible (FA2 à FA8) du côté dudit potentiel d'alimentation (VCC) et une sortie de potentiel provenant dudit inverseur (INV1).

7. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel lesdits circuits détecteurs de fusible coupé (FK2 à FK8) sont respectivement connectés à un second élément et aux éléments suivants desdits éléments fusibles (FA2 à FA8) provenant dudit potentiel d'alimentation (VCC).

8. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel lesdits circuits détecteurs de fusible coupé (FK2 à FK8) interrompent le courant d'alimentation dudit circuit d'écriture/lecture (YS1 à YS8 et SA1 à SA8) auquel est alloué un élément coupé desdits éléments fusibles (FA1 à FA8).

9. Circuit mémoire à semiconducteur selon la revendication 3, dans lequel ledit circuit de programme (PR1) comprend :

une résistance (R1) connectée entre ledit élément fusible de commutation (FAP) et ledit potentiel de masse ;

un premier inverseur (INV3) connecté à un noeud reliant ledit élément fusible de commutation (FAP) et ladite résistance (R1) ; et

un second inverseur (INV4) connecté en série audit premier inverseur (INV3).

10. Circuit mémoire à semiconducteur selon la revendication 1, dans lequel lesdits circuits de redondance de décalage (SF1 à SF8) comprennent chacun :

un premier circuit de commutation (TF1) qui est conducteur lorsque ledit élément fusible (FA1 à FA8) alloué audit circuit de redondance de décalage (SF1 à SF8) est coupé et est non conducteur lorsque ledit élément fusible (SF1 à SF8) n'est pas coupé ; et

un second circuit de commutation (TF2) qui est non conducteur lorsque ledit élément fusible (SF1 à SF8) alloué audit circuit de redondance de décalage est coupé et est conducteur lorsque ledit élément fusible (SF1 à SF8) n'est pas coupé.

FIG. 1

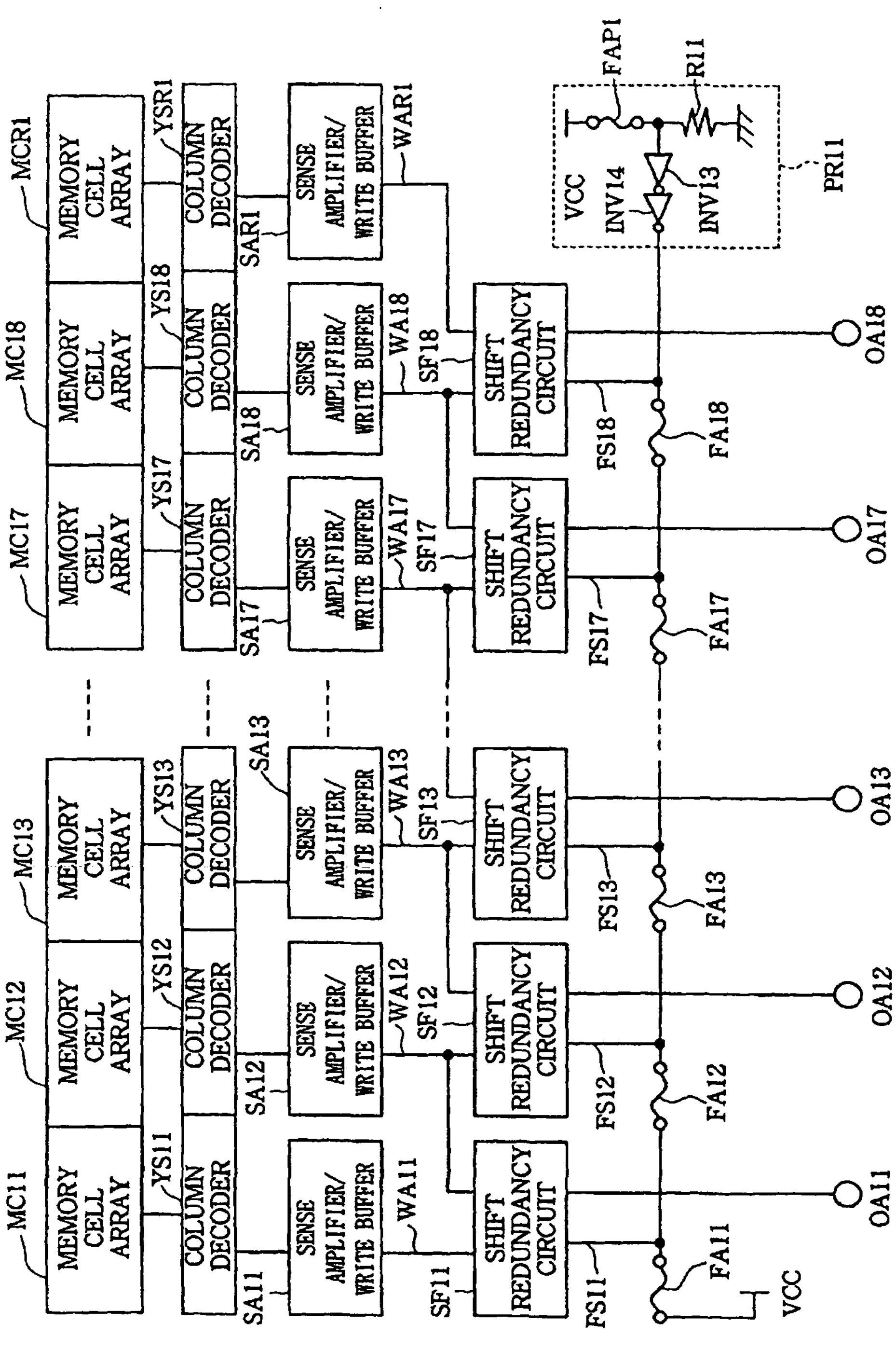

MC11
MEMORY CELL ARRAY
MC12
MEMORY CELL ARRAY
MC13
MEMORY CELL ARRAY
MC17
MEMORY CELL ARRAY
MC18
MEMORY CELL ARRAY
MCR1
MEMORY CELL ARRAY
YS11
YS12
YS13
YS17
YS18
YSR1
COLUMN DECODER
SA11
SA12
SA13
SA17
SA18
SAR1
SENSE AMPLIFIER/ WRITE BUFFER
WA11
WA12
WA13
WA17
WA18
WAR1
SF11
SF12
SF13
SF17
SF18
SHIFT REDUNDANCY CIRCUIT
FS11
FS12
FS13
FS17
FS18
FA11
FA12
FA13
FA17
FA18
VCC
OA11
OA12
OA13
OA17
OA18
FAP1
R11
INV14
INV13
PR11

FIG. 2

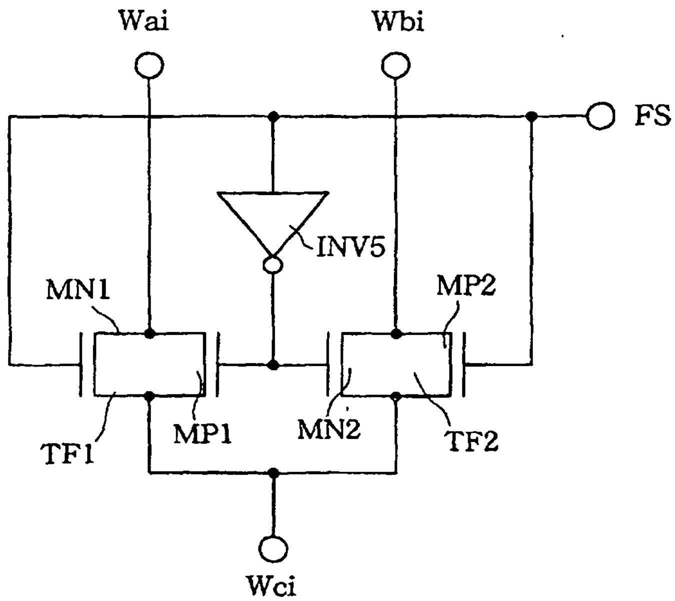

Wai
Wbi
FS
INV5
MN1
MP2
TF1
MP1
MN2
TF2
Wci

FIG. 3

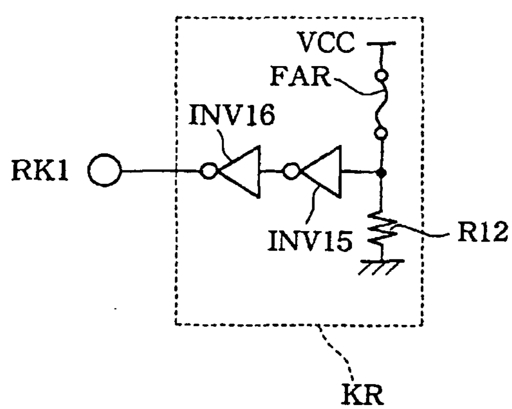

VCC
FAR
INV16
RK1
INV15
R12
KR

FIG. 4

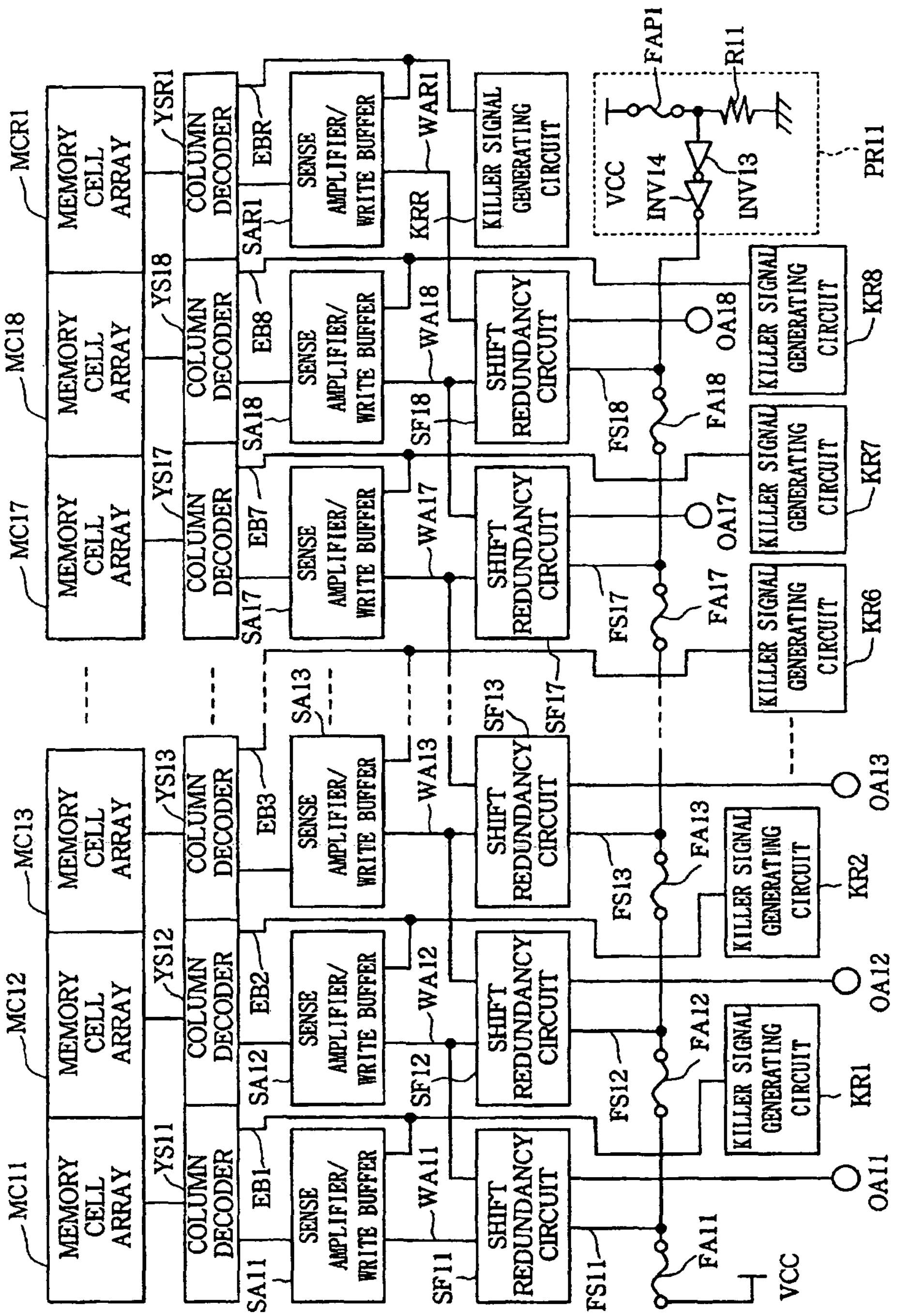
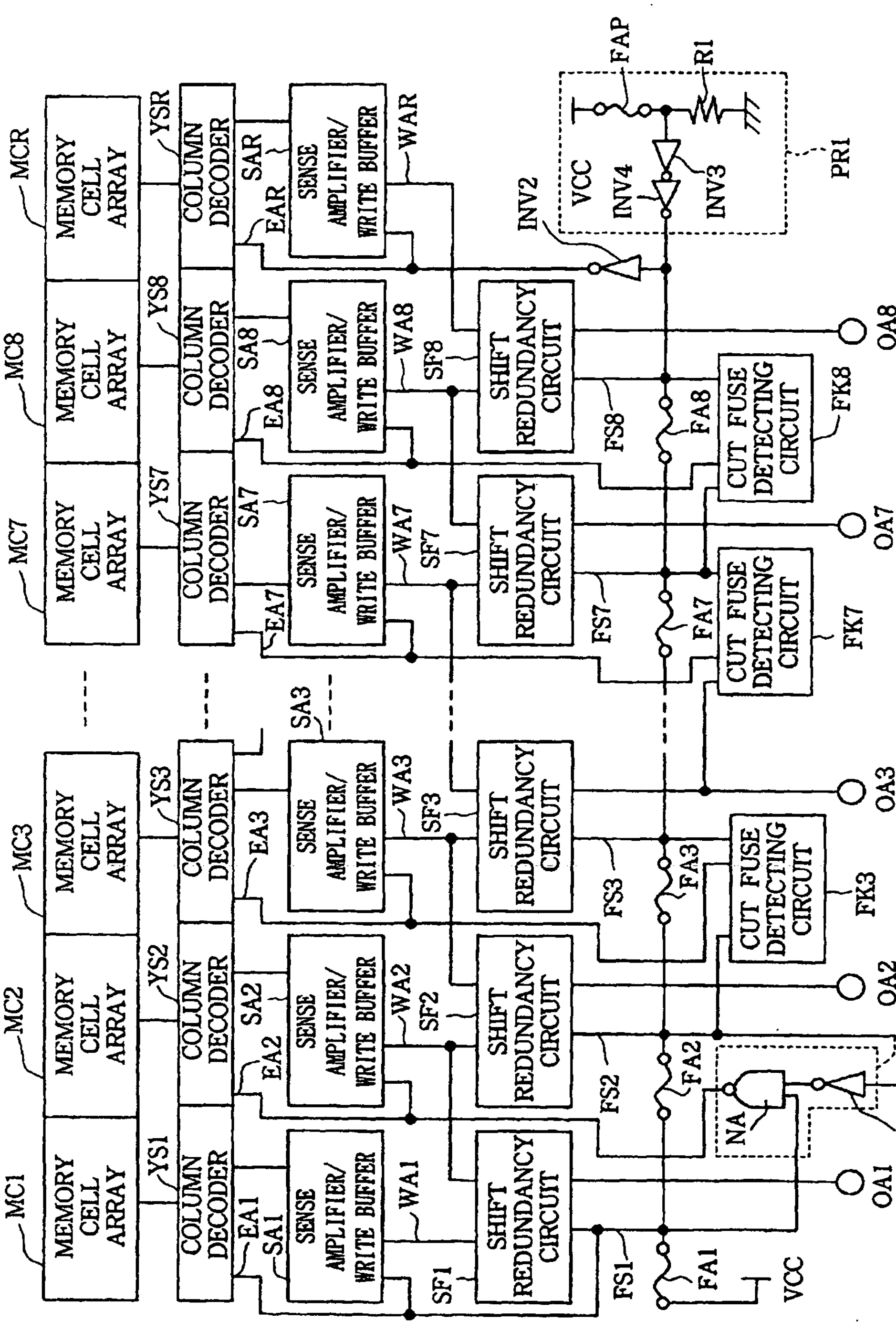

MEMORY CELL ARRAY
COLUMN DECODER
SENSE AMPLIFIER/WRITE BUFFER
SHIFT REDUNDANCY CIRCUIT
KILLER SIGNAL GENERATING CIRCUIT
MC11
MC12
MC13
MC17
MC18
MCR1
YS11
YS12
YS13
YS17
YS18
YSR1
SA11
SA12
SA13
SA17
SA18
SAR1
EB1
EB2
EB3
EB7
EB8
EBR
WA11
WA12
WA13
WA17
WA18
WAR1
SF11
SF12
SF13
SF17
SF18
FS11
FS12
FS13
FS17
FS18
FA11
FA12
FA13
FA17
FA18
OA11
OA12
OA13
OA17
OA18
KR1
KR2
KR6
KR7
KR8
KRR
VCC
FAP1
R11
INV13
INV14
PR11

FIG. 5


MEMORY CELL ARRAY
COLUMN DECODER
SENSE AMPLIFIER/ WRITE BUFFER
SHIFT REDUNDANCY CIRCUIT
CUT FUSE DETECTING CIRCUIT
MC1
MC2
MC3
MC7
MC8
MCR
YS1
YS2
YS3
YS7
YS8
YSR
EA1
EA2
EA3
EA7
EA8
EAR
SA1
SA2
SA3
SA7
SA8
SAR
WA1
WA2
WA3
WA7
WA8
WAR
SF1
SF2
SF3
SF7
SF8
FS1
FS2
FS3
FS7
FS8
FA1
FA2
FA3
FA7
FA8
FK2
FK3
FK7
FK8
OA1
OA2
OA3
OA7
OA8
NA
INV1
INV2
INV3
INV4
VCC
FAP
R1
PR1